REMARKS

Claims 1-9, 11, 12, 14, and 15 are pending and under consideration. Claims 1-5, 7, 8, 9, 11, 12, and 14 have been amended. Claim 15 is added herein. Support for the amendments to the claims may be found in the claims as originally filed. Further reconsideration is requested based on the foregoing amendment and the following remarks.

Response to Arguments:

The Applicants appreciate the consideration given to their arguments. The Applicants, however, are disappointed that their arguments were not found to be persuasive.

The Advisory Action mailed March 31, 2006 responded to the argument that Kaiser shows no "means for creating an inter-drawing connection diagram file" in section 2 at page 2 by asserting that:

> Kaiser discloses a means for (fig. 4, num. 38 or "schematic capture package" in col. 3, line 36) creating ("created" in col. 3, line 34) an inter-drawing connection diagram file (as shown by the connections via the arrows within fig. 4, num. 38 or as shown in fig. 1, where each sheet of fig. 1 is connected to other sheets via a solid or dashed line.).

This interpretation of Kaiser is submitted to be incorrect. Kaiser is directed to a critical path, or timing, analyzer as described at column 4, line 4. Fig. 4 shows pseudo-code and source code data structures, not means for creating an inter-drawing connection diagram file, contrary to the assertion in the Advisory Action. In particular, as described at column 6, lines 61-67:

> Referring now to FIG. 4, both the pseudo-code and source code assume the existence of three data structures: a graphics structure 36, a connectivity structure 38, and a path structure 40. The graphics structure 36 and connectivity structure 38 are generated by means such as a schematic editor previously described in response to the input from the designer.

The lines connecting the graphics structure 36, the connectivity structure 38, and the path structure 40 show their various inputs and outputs, not an inter-drawing connection diagram. In particular, as described at column 6, lines 67 and 68, continuing at column 7, lines 1 and 2:

> A transform program 42 within the schematic editor transforms the data from the graphics structure 36 into data for the connectivity structure 38.

Kaiser is interested in providing a critical path analyzer, not an inter-drawing connection diagram. In particular, as described at column 6, lines 67 and 68, continuing at column 7, lines 2-7:

> A critical path analyzer 44 communicates with the connectivity structure 38 to define paths and determine which paths are critical. Path means such as path

> structure 40 then accept data from the analyzer 44 defining critical signal paths and stores the paths by reference to input-output pin pairs.

Therefore, to assert that Kaiser shows a "means for creating an inter-drawing connection diagram file," when he is really after a critical path analyzer, is submitted to be without basis.

The Advisory Action mailed March 31, 2006 responded to the argument that Kaiser describes no "relations of mutual connections between a plurality of drawings" in section 3 at pages 2 and 3 by asserting that:

> Kaiser describes relations of mutual connections (as shown by either a dashed or solid line between the rectangles that are labeled as "SHEET") between a plurality of drawings (where each sheet has a drawing).

This interpretation of Kaiser is also submitted to be incorrect. The lines between the drawing rectangles in Fig. 1 of Kaiser, rather, indicate a hierarchy of the drawings, not relations of mutual connections. In particular, as described at 3, lines 32, 33, and 34:

> Referring now to FIG. 1 of the drawings, there is shown a hierarchial view of schematic sheets for a circuit design.

The hierarchy of drawings in Kaiser, in particular, indicates a progression from general to specific, not relations of mutual connections. In particular, as described at column 3, lines 40-47:

> With a schematic editor, a designer can create a hierarchy of design levels, with each level representing a different level of hardware modeling. For example, in FIG. 1, the top level of schematic sheets is the most general design. The lower level is more specific, with each sheet corresponding to an individual component which the designer wishes to model.

Therefore, to assert that Kaiser "describes relations of mutual connections between a plurality of drawings," when he really shows a hierarchy between the drawings, is submitted to be without basis.

Finally, the Advisory Action mailed March 31, 2006 responded to the argument that Kaiser shows no "means for indicating, on one screen, a plurality of the drawings miniaturized according to the description in the inter-drawing connection diagram file which has been created" in section 4 at page 3 by asserting that:

> Kaiser does have an element (fig. 2, num. 34a) corresponding to means for indication, on one screen, a plurality of the drawings miniaturized (fig. 2, num. 34a includes at least fig. 2, num 22 as shown in the middle left side of fig. 2, num. 34a as a "functional block" in col. 5, line 63 which corresponds to the claimed "drawings miniaturized") according to the description in the inter-drawing

> connection diagram file (of fig. 1 where ADD-DET SHEET 1 corresponds to fig. 2, num 34a and DECODE SHEET 1 corresponds to fig. 2, numerals 34b shown as individual elements and in fig. 2, num 34a as a functional block) which has been created.

This interpretation of Kaiser is also submitted to be incorrect. Symbol 22 in Fig. 2 is a symbol, not a drawing miniaturized or a functional block, contrary to the assertion in the Advisory Action. Symbol 22, rather, is displayed in the display portion 18b adjacent to the path portion to assist the user in determining that this chip is the source of the path portion, as described at column 5, lines 4-7:

> To assist the user in determining that this chip is the source of the path portion, a symbol 22 for the component is displayed in the display portion 18b adjacent to the path portion.

Furthermore, view sheet windows 34a and 34b show different levels of design of the same decoder chip, not "means for indicating, on one screen, a plurality of the drawings miniaturized according to the description in the inter-drawing connection diagram file which has been created." In particular, as described at column 5, lines 57-66:

> In FIG. 2, view sheet window 34a shows sheet 1 of ADD_DET that includes the first and final path portions of path 2. View sheet window 34b shows sheet 1 of DECODE and displays the internal gate circuitry of the decoder chip, represented by symbol 22. The decoder chip, it can now be seen, is represented in sheet 1 of ADD_DET as a functional block. At the lower design level in sheet 1 of DECODE, the individual gates, input pins, and output pins of the decoder chip are displayed.

Therefore, to assert that Kaiser ""means for indicating, on one screen, a plurality of the drawings miniaturized according to the description in the inter-drawing connection diagram file which has been created," when he really shows different levels of design of the same decoder chip, is submitted to be without basis. Further reconsideration is thus requested.

Objections to the Specification:

The Specification has been objected to for various informalities. Appropriate corrections were made. The Examiner's suggestions are appreciated. The reference to Fig. 10 at page 11, line 28, however, is submitted to be correct, so that was not changed. Fig. 10, in particular, is based on the inter-drawing connection diagram depicted in Fig. 9. Fig. 11 includes 4 drawings A to D, and Fig. 12 is derived from Fig. 11 based on the inter-drawing connection diagram. Withdrawal of the objection is earnestly solicited.

Claim Rejections - 35 U.S.C. § 102:

Claims 1-8 and 14 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,970,664 to Kaiser et al. (hereinafter "Kaiser"). The rejection is traversed to the extent it would apply to the claims as amended.

Several embodiments of the present invention may improve the visibility of connections among logical drawing sheets. Kaiser, and Figs. 2-22 of Kaiser, in particular, cannot improve the visibility of connections among logical drawing sheets because Figs. 2-22 are not connected with each other as logical drawings, as described above. In order to define the invention more clearly, the third clause of claim 1 has been amended to recite, "miniaturized drawing sheets are connected by nets," a feature most decidedly not present in Kaiser.

The second clause of claim 1, furthermore, recites:

> A means for creating an inter-drawing diagram file which describes interrelation in a plurality of drawing sheets.

Kaiser neither teaches, discloses, nor suggests "a means for creating an inter-drawing diagram file which describes interrelation in a plurality of drawing sheets," as recited in claim 1. In Kaiser, rather, the screen display includes a path context window for displaying a signal path, not "a plurality of drawing sheets," as recited in claim 1. In particular, as described in the Abstract of Kaiser:

> A screen display includes a path context window for displaying a signal path in its entirety apart from the schematic sheets on which the path portions appear. The window contains multiple display portions each graphically displaying a path portion appearing on a separate schematic sheet.

Since, in Kaiser, the screen display includes a path context window for displaying a signal path, Kaiser cannot show "a means for creating an inter-drawing diagram file which describes interrelation in a plurality of drawing sheets," as recited in claim 1.

The third clause of claim 1 recites:

> Inter-drawing indication means for indicating, on one screen, a plurality of the miniaturized drawing sheets, said miniaturized drawing sheets are connected by nets, according to the description in the inter-drawing diagram file which has been created.

Since Kaiser neither teaches, discloses, nor suggests "a means for creating an inter-drawing diagram file which describes interrelation in a plurality of drawing sheets," as discussed above, Kaiser cannot show "inter-drawing indication means for indicating, on one screen, a plurality of

the miniaturized drawing sheets, said miniaturized drawing sheets are connected by nets, according to the description in the inter-drawing diagram file which has been created," as recited in claim 1, either. Claim 1 is submitted to be allowable. Withdrawal of the rejection of claim 1 is earnestly solicited.

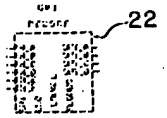
Claims 2 through 8 depend from claim 1 and add further distinguishing elements. Claims 2 through 8 are thus also submitted to be allowable. Withdrawal of the rejection of claims 2 through 8 is also earnestly solicited.

Claim 14:

The second clause of claim 14 recites:

> A hierarchic symbol drawing means for drawing by dividing said hierarchic symbols.

Kaiser neither teaches, discloses, nor suggests "a hierarchic symbol drawing means for drawing by dividing said hierarchic symbols," as recited in claim 14. In Kaiser, rather, symbol 22, to which the final Office Action analogizes the hierarchic symbol recited in claim 14, is not divided, as may be seen in the excerpt from Fig. 2 of Kaiser shown below:



Since, in Kaiser, symbol 22 is undivided, Kaiser shows no "hierarchic symbol drawing means for drawing by dividing said hierarchic symbols," as recited in claim 14.

Furthermore, in Kaiser, symbol 22 is for the component displayed in the display portion 18b adjacent to the path portion, not a "hierarchic symbol drawing means for drawing by dividing said hierarchic symbols," as recited in claim 14. In particular, as described at column 5, lines 4-7 of Kaiser:

> To assist the user in determining that this chip is the source of the path portion, a symbol 22 for the component is displayed in the display portion 18b adjacent to the path portion.

Since, in Kaiser, symbol 22 is for the component displayed in the display portion 18b adjacent to the path portion, Kaiser has no need for a "hierarchic symbol drawing means for drawing by dividing said hierarchic symbols," as recited in claim 14. Claim 14 is submitted to be allowable. Withdrawal of the rejection of claim 14 is earnestly solicited.

Claims 9, 11 and 12:

Claims 9, 11 and 12 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,218,551 to Agrawal et al. (hereinafter "Agrawal"). The rejection is traversed to the extent it would apply to the claims as amended.

Claim 9 recites:

> Symbol selecting means for selecting symbols to be moved and positions to which the selected symbols are to be moved.

Claim 9 is a so-called "means-plus-function" claim within the meaning of 35 U.S.C. §112, sixth paragraph. As such, claim 9 ought to be "construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof," as provided in 35 U.S.C. §112, sixth paragraph. Agrawal is submitted to show no "symbol selecting means for selecting symbols to be moved and positions to which the selected symbols are to be moved," corresponding to structure, material, or acts described in the *present* specification, or equivalents thereof, as required by 35 U.S.C. §112, sixth paragraph. In Agrawal, rather, symbols are moved automatically, at random. In particular, as described at column 17, lines 55-59:

> The segments that are chosen to be interchanged in the move between precincts are randomly chosen but must be within a move class. A move class is a group of segments assigned to precincts which are within a predefined distance from each other.

Since, in Agrawal, symbols are moved automatically, at random, Agrawal shows no "symbol selecting means for selecting symbols to be moved and positions to which the selected symbols are to be moved," corresponding to structure, material, or acts described in the *present* specification, or equivalents thereof, as recited in claim 9. Claim 9 is submitted to be allowable. Withdrawal of the rejection of claim 9 is earnestly solicited.

Claims 11 and 12 depend from claim 9 and add further distinguishing elements. Claims 11 and 12 are thus also submitted to be allowable. Withdrawal of the rejection of claims 11 and 12 is also earnestly solicited.

New Claim 15:

Claim 15 depends from claim 1 and adds further distinguishing elements. Claim 15 is thus also believed to be allowable, for at least those reasons discussed above with respect to the rejection of claim 1.

Allowable Subject Matter:

The Applicant acknowledges with appreciation the indication of allowable subject matter.

Conclusion:

Accordingly, in view of the reasons given above, it is submitted that all of claims 1-9, 11, 12, 14, and 15 are allowable over the cited references. Allowance of all claims 1-9, 11, 12, 14, and 15 and of this entire application is therefore respectfully requested.

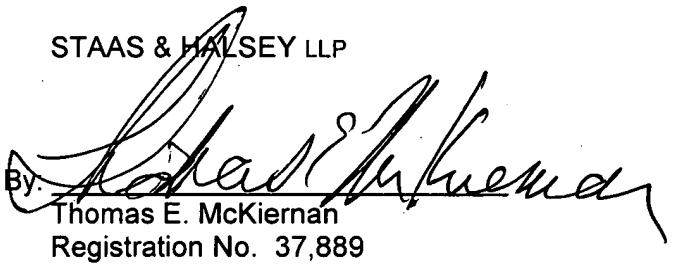
If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 12MY06

By: 
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